

Clean Set of Amended Claims

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1. (Amended) A test circuit for a microcontroller unit, comprising:  
an input circuit that consists of,  
a first pin receiving a first signal, and  
a second pin receiving a second signal; and  
a test signal generating circuit that generates a test signal in response to a  
logical combination of the first signal and the second signal.
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2. (Amended) The circuit of claim 1, wherein the test signal generating circuit  
comprises:  
a logic circuit that logically processes the first signal and the second signal;  
a counter that is enabled and disabled based on an output signal from the  
logic circuit, wherein the counter uses the second signal as a counting signal when  
enabled; and  
a decoder that outputs the test signal when a count value from the counter  
reaches a prescribed count value.
3. (Amended) The circuit of claim 2, wherein the counter is disabled and reset  
when the output signal from the logic circuit is a low level.

5. (Amended) The circuit of claim 2, comprising:

a test mode related circuit operated by the first signal and the second signal;

and

an internal circuit that enters a test mode in accordance with the test signal

from the test signal generating circuit, wherein the counter counts a plurality of prescribed values of the second signal.

<sup>10</sup>/<sub>8</sub>

(Amended) A microcontroller unit having a test mode setup circuit, the test mode setup circuit comprising:

a clock pin that receives a clock signal;

a reset pin that receives a reset signal;

a test mode counter that is set and reset based on the clock signal and the reset signal, wherein the test mode counter counts the reset signal; and

a decoder that receives a count value from the test mode counter and activates a test mode flag when the count value reaches a prescribed value.

<sup>14</sup>/<sub>12</sub>

(Amended) The microcontroller unit of claim <sup>10</sup>/<sub>8</sub>, wherein the test mode setup circuit comprises:

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an input circuit that consists of first and second pins, wherein the first pin  
ay is the clock pin and the second pin is the reset pin; and

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an OR gate ORing the clock signal and the reset signal.

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**B.** Please add new claims 18-24 as follows:

<sup>9</sup>  
~~18.~~ (New) The circuit of claim 1, wherein the test circuit does not have a test signal input terminal.

<sup>9</sup>  
~~19.~~ (New) The circuit of claim 1, wherein the test circuit does not receive a separate enable test signal.

20. (New) The circuit of claim <sup>17</sup>~~15~~, wherein the test mode counter counts a plurality of prescribed values of the reset signal.

as  
21. (New) The circuit of claim <sup>17</sup>~~15~~, further comprising a test input circuit that consists of first and second pins, wherein the first pin is the clock pin and the second pin is the reset pin.

<sup>23</sup>  
~~22.~~ (New) A test mode setup circuit, the test mode setup circuit comprising:  
first pin means for receiving a first signal; and  
second pin means for receiving a second signal;

counting means for counting that is set and reset based on the first signal and  
5 the second signal, wherein the counting means counts the second signal; and

decoding means for receiving a count value from the counting means and  
activating a test mode flag when the count value reaches a prescribed value.

<sup>24</sup>  
~~23~~. (New) The circuit of claim <sup>23</sup>~~22~~, further comprising:

AS test mode means operated by the first signal and the second signal that  
outputs a test signal based on the test mode flag; and

logic means for logically processing the first signal and the second signal to  
5 generate a control signal for the counting means:

<sup>22</sup>  
~~24~~. (New) The circuit of claim 21, wherein the counting means counts a  
plurality of prescribed values of the second signal.

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